EICoM
ELECTRICAL COMPUTER MECHATRONICS

تقدم لجنة

ملخص لمادة:

منطق رقمي

جزيل الشكر للطالب:

حمزة اسماعيل

Digital logic and Digital Electronics:

* Digital logic :-

* Number Systems :-

1- Binary system : النظام الثنائي
base (2, B) , element (0,1).

2- Decimal system النظام العشري
base (10) , element (0-9).

3- Octal system . النظام الثماني
base (8, O) , element (0-7).

4- Hexadecimal system
base (16, H) , element (0-9, A-F).

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* least and most significant Bit :-

least significant Bit (LSB).
Most significant Bit (MSB).

10100 11
MSB ← → LSB

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* Bit = 0 or 1.
Nibble = 4 bits.
Byte = 8 bits.
Word = 2 Byte = 16 bits.

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* Conversion from Binary and Octal and hexadecimal to Decimal :-

! ⇒ من اي نظام للنظام العشري نضرب بأساس النظام .

1- Conversion from Binary to Decimal :-

$10111_{(2)}$ → Decimal.

$10111_{(2)} = 1*2^4 + 0*2^3 + 1*2^2 + 1*2^1 + 1*2^0$

$= 16 + 4 + 2 + 1 = 23_{(10)}$.

$1100.101_{(2)}$ → Decimal.

$1100.101_{(2)} = 1*2^3 + 1*2^2 + 1*2^{-1} + 1*2^{-3}$

$= 8 + 4 + \frac{1}{2} + \frac{1}{8} = 12.625_{(10)}$

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* Conversion from Binary and Octal and hexadecimal to Decimal :-

2- Conversion from Octal to Decimal

$2371_{(8)}$ → Decimal.

$2371_{(8)} = 2*8^3 + 3*8^2 + 7*8^1 + 1*8^0$.

$= 1024 + 192 + 56 + 1$

$= 1273_{(10)}$

3- Conversion from Hexadecimal to Dec :-

$ABED_{(16)}$ → Decimal.

$ABED_{(16)} = A*16^3 + B*16^2 + E*16^1 + D*16^0$.

$= 40960 + 2816 + 208 + 13$

$= 44013_{(10)}$

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* Conversion from Decimal to Binary and Octal and Hexadecimal :-

⇒ من النظام العشري لأي نظام نضرب او نقسم

Integer → نقسم ، fraction → نضرب

1- Conversion from Decimal to Binary :-

$6_{(10)}$ ⇒ Binary.

6	
3	0 → LSB
1	1
0	1 → MSB

$6_{(10)} = 110_{(2)}$

$0.125_{(10)}$ ⇒ Binary.

0.125	
0.25	0
0.5	0
0	1

$0.125_{(10)} = 0.001_{(2)}$

2- Conversion from Decimal to Octal

$812_{(10)}$ ⇒ Octal

812	
101	4
12	5
1	4
0	1

$812_{(10)} = 1454_{(8)}$

$0.0625_{(10)}$ ⇒ Octal

0.0625	
0.5	0
0	4

$0.0625_{(10)} = 0.04_{(8)}$

3- Conversion from Decimal

171 ⇒ Hexadecimal.

1) $171_{(10)}$

171	
10	11 → B

$171_{(10)} = AB_{(16)}$.

* Digital logic and Digital Electronic

* Digital logic :-

* Number Systems :-

* Conversion from Binary to Octal and Vica Versa :-

$101110_{(2)} \Rightarrow$ Octal.

(4 2 1) (4 2 1)

$101110_{(2)} = 56_{(8)}$.

$001010.1101_{(2)} \Rightarrow$ Octal

$1010.1101_{(2)} = 12.64_{(8)}$

$37_{(8)} \Rightarrow$ Binary.

$37_{(8)} = 011\,111_{(2)}$.

Binary	Octal
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

(4 2 1)

* Conversion from Binary to Hexadecimal and Vica Versa :-

$0001.1000_{(2)} \Rightarrow$ Hexadecimal

(8 4 2 1)

$1.1_{(2)} = 1.8_{(16)}$

$10111.111_{(2)} \Rightarrow$ Hexadecimal

(8 4 2 1)

$10111.111_{(2)} = 17.E_{(16)}$

$CAB.BEE \Rightarrow$ Binary.

12 10 11 11 14 14

$= 1100\,1010\,1011.1011\,1110\,1110_{(2)}$

$ABED_{(16)} \Rightarrow$ Binary.

10 11 14 13

$ABED_{(16)} = 1010\,1011\,1101\,1101_{(2)}$

Binary	Hexa.
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

8421

* Conversion from Hexadecimal to Octal and Vica Versa :-

$273_{(8)} = 010\,111\,011_{(2)} = BB_{(16)}$

$B.A_{(16)} = 1011.1010_{(2)} = 13.5_{(8)}$

* Binary Coded Decimal (BCD) :-

$29_{(10)} \Rightarrow$ BCD.

$29_{(10)} = \underbrace{0010}_{\text{BCD Digit.}}\,\underbrace{1001}_{\text{(BCD)}}$

$49_{(10)} \Rightarrow$ BCD.

$49_{(10)} = \underbrace{0100}_{\text{BCD Digit.}}\,\underbrace{1001}_{\text{BCD.}}$

$01110100_{(BCD)} \Rightarrow$ Decimal

$01110100_{(BCD)} = 74_{(10)}$

Binary	Decimal
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9.

* Gray Code :-

$42_{(10)} \Rightarrow$ Gray Code.

$42_{10} = \underbrace{0110}_{\text{Gray digit.}}\,\underbrace{0011}_{(10)}$

$00100111_{(Gray)} \Rightarrow$ Decimal

$0010\,0111_{Gray} = 35_{10}$

Gray Code	Decimal
0000	0
0001	1
0011	2
0010	3
0110	4
0111	5
...	...
	15

بعد كده

* Complement :- (2 kinds)

1- One's complement (1's comp).

نعكس ⇒ 0 → 1 , 1 → 0.

Ex:- $0110_{(2)} \xrightarrow{1\text{'s comp}} 1001_{(2)}$

2- Two's complement (2's comp).

2's comp = 1's comp + 1.

Ex:- $001101_{(2)} \xrightarrow{2\text{'s comp}} 110011_{(2)}$.

$00111000_{(2)} \xrightarrow{2\text{'s comp}} 11001000_{(2)}$

* Conversion from Hexadecimal to Octal and Vica Versa :-

$273_{(8)} = 010\,111\,011_{(2)} = BB_{(16)}$

$B.A_{(16)} = 1011.1010_{(2)} = 13.5_{(8)}$

* Digital logic and Digital Electronics :-

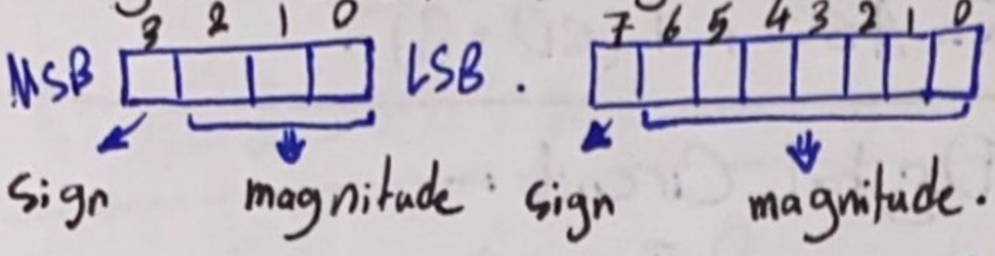
* Digital logic :-

* Representation of number in binary :-

1- Sign - Magnitude representation :-

Register : 7 6 5 4 3 2 1 0

Register 4 bit , Register 8 bits .



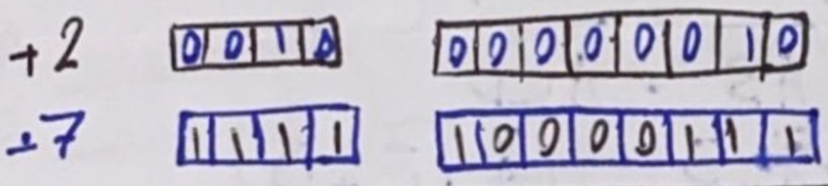
maxumum and minumum number of bits = $\pm (2^{n-1} - 1)$

n = 4 bits ⇒ max / min = ± 7 .

n = 8 bits ⇒ max / min = ± 127

Sign :

Positive → 0 . negative → 1 :



* Representation of number in binary :-

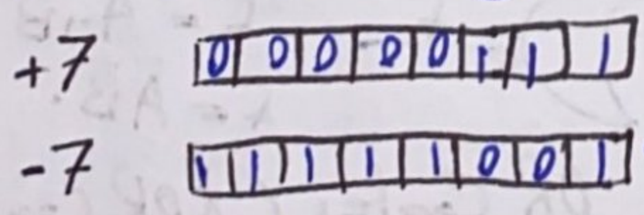
2- Ones Complement representation :-

- Positive number ⇒ stay the same.
- Negative number ⇒ you need 1's Comp

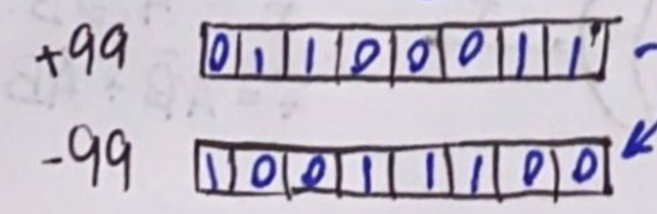
3- Two's Complement representation :-

- Positive number ⇒ stay the same.
- Negative number ⇒ you need 2's Comp

Ex :- represent using 2's comp. represent.



Ex :- represent using 1's comp. represent... :-



* Representation of number in binary :-

4- Floating Point representation :-

هو تمثيل الأرقام الكبيرة والصغيرة جداً .

مش > اخل

* Ranges :-

1- Sign - Magnitude representation

Positive number ⇒ $\pm (2^{n-1} - 1)$.

negative number

2- One's Complement representation

Positive number ⇒ $\pm (2^{n-1} - 1)$.

negative number

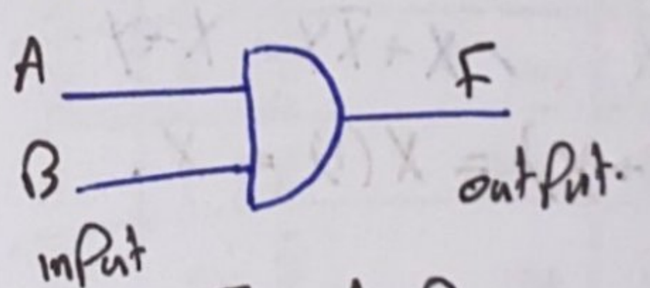
3- Two's complement representation

Positive number ⇒ $\pm (2^{n-1} - 1)$

negative number ⇒ $(-2^{n-1} \rightarrow 2^{n-1} - 1)$

* Logic Gates :-

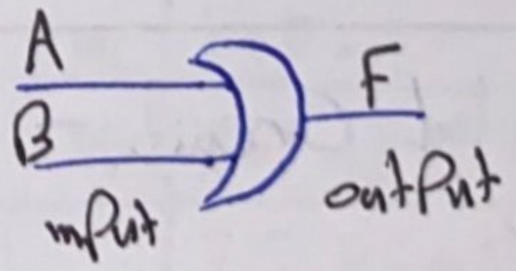
1 AND Gates :-



F = A . B

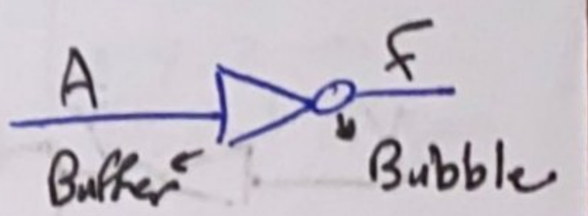
2- OR Gates :-

F = A + B



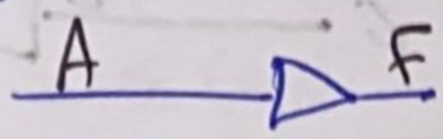
3- Inverter (Not) Gates :-

F = A' ↝ Compl



4- Buffer Gates :-

F = A



Digital logic and Digital Electronics :-

* Logic Gates :-

* Boolean Theorems and Properties :-

1- Closure with respect to "+, ." operator

2- $X+0=X$, $X+1=1$

$X.1=X$, $X.0=0$

3- Commutative تبديلي

$X+y=y+X$, $X.y=y.X$

4- Distributive توزيعي

$X.(y+z)=X.y+X.z$

$X+(y.z)=Xy+Xz$

5- $X+\bar{X}=1$, $X.\bar{X}=0$

$y+\bar{y}=1$, $y.\bar{y}=0$

* Demorgan Theorem :-

1- $(X+y)' = \overline{(X+y)} = \bar{X}.\bar{y}$

2- $(X.y)' = \overline{(X.y)} = \bar{X}+\bar{y}$.

* Absorption Theorem :-

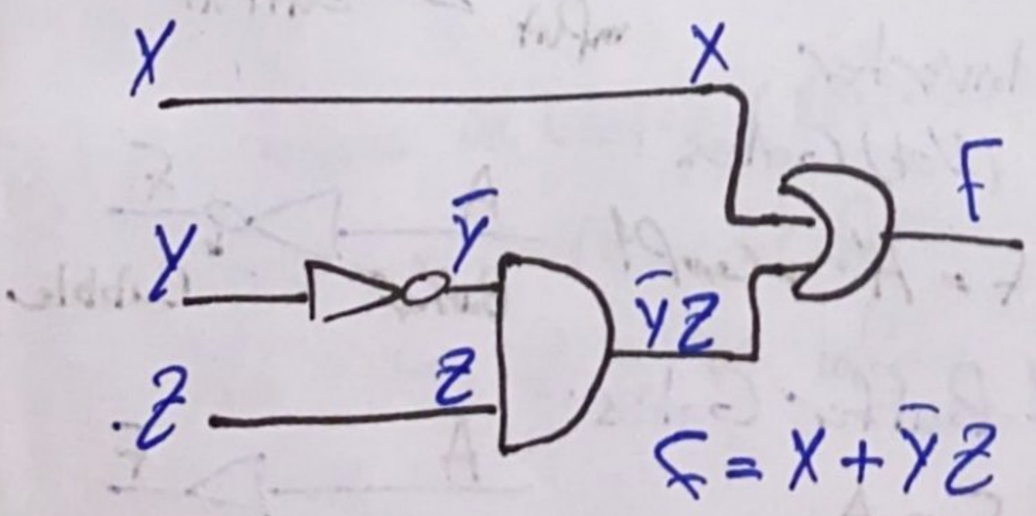
1- $X+Xy=X$, $X+\bar{X}y=X+y$.

Proof :- $X(1+y)=X(1)=X$.

2- $X(X+y)=X$

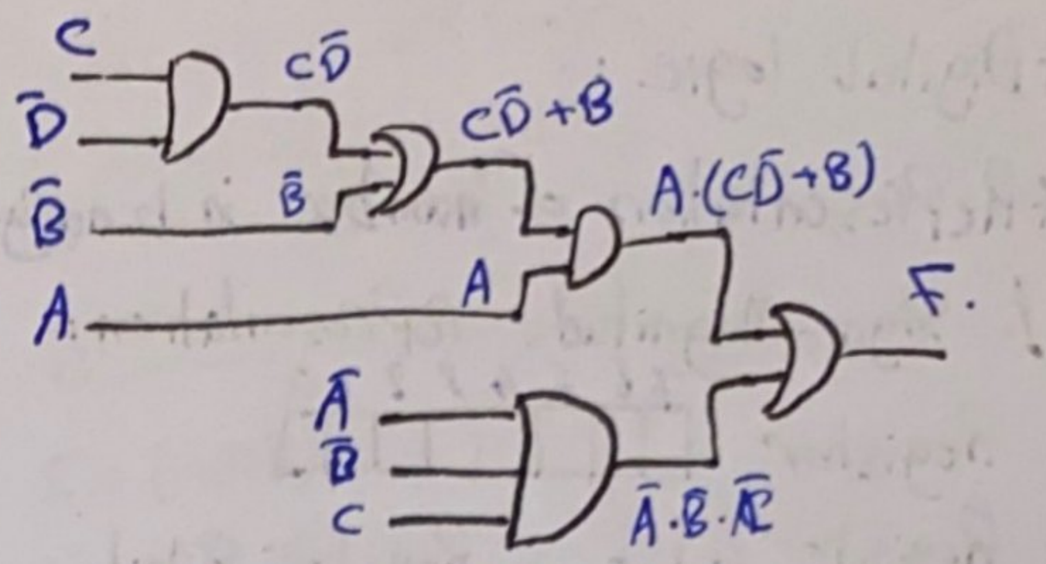
Proof :- $X+Xy=X(1+y)=X$

* Digital Circuit :-



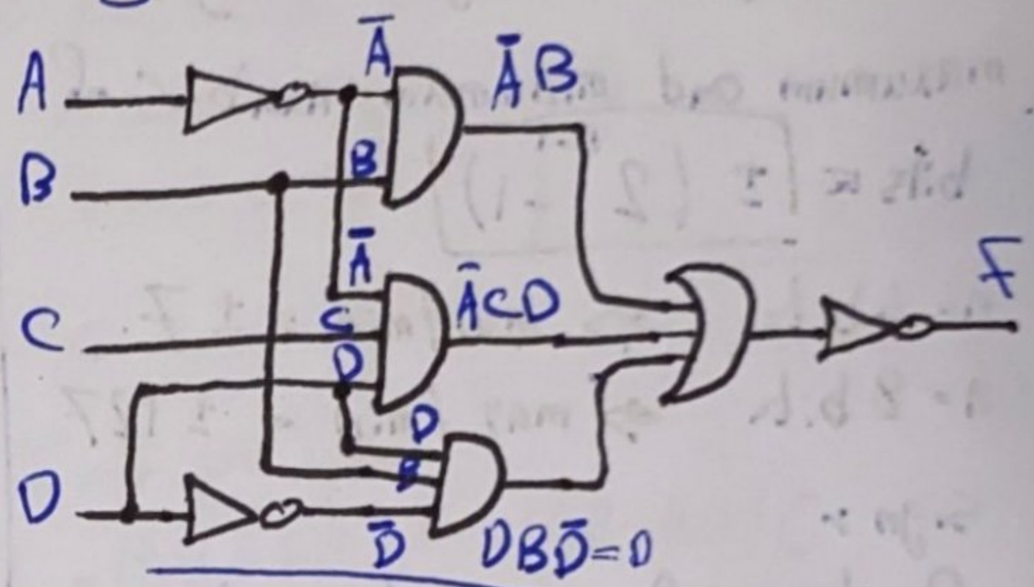
$F=X+\bar{Y}Z$

* Digital Circuit :-



$F=\bar{A}\bar{B}\bar{C}+A.(C\bar{D}+B)$

* Digital Circuit :-



$F=(\bar{A}B+\bar{A}CD)$

$F=\overline{\bar{A}B}\cdot\overline{\bar{A}CD}$

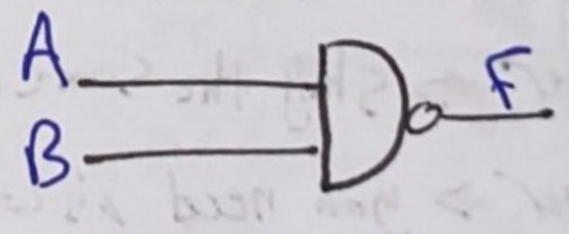
$=(\bar{\bar{A}}+\bar{B})\cdot(\bar{\bar{A}}+\bar{C}+\bar{D})$

$=(A+\bar{B})\cdot(A+\bar{C}+\bar{D})$

$F=AA+A\bar{C}+A\bar{D}+A\bar{B}+\bar{C}\bar{B}+\bar{B}\bar{D}$

* Logic Gates :-

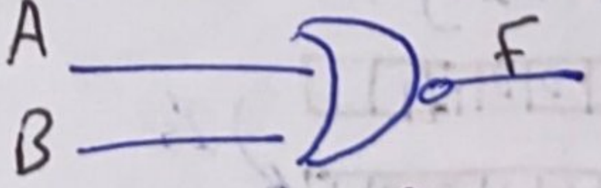
5- NAND Gates (AND Not Gates) :-



$F=\overline{AB}$

$F=\bar{A}+\bar{B}$.

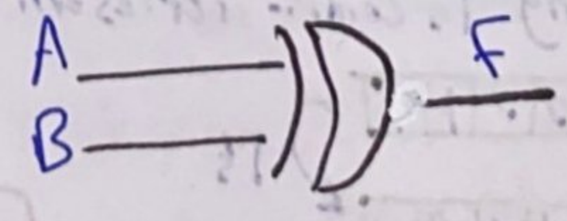
6- NOR Gates (OR Not Gates) :-



$F=\overline{A+B}$

$F=\bar{A}\bar{B}$.

7- Exclusive OR Gates (XOR Gates)



$F=A\oplus B$

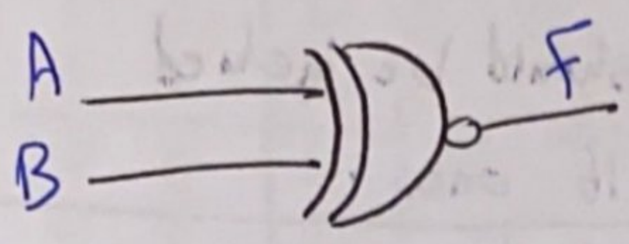
$F=A\bar{B}+\bar{A}B$.

* Digital logic and Digital Electronics:-

* Digital logic :-

* logic Gates :-

8- Exclusive NOR Gates (XNOR):-



$F = A \odot B$

$F = \overline{A \oplus B}$

$F = A \odot B = \bar{A}\bar{B} + AB$.

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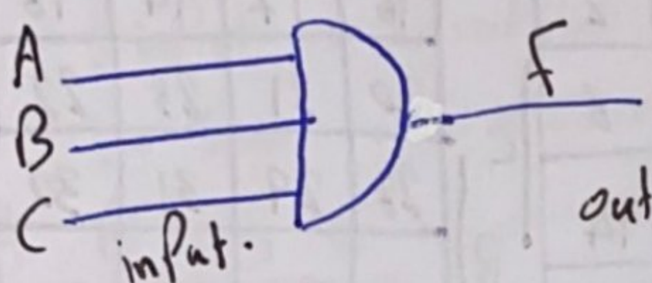
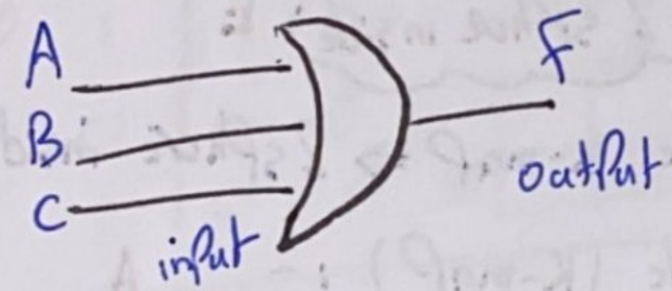
* logic Gates Three Input Gates :-

1- AND Gates :-



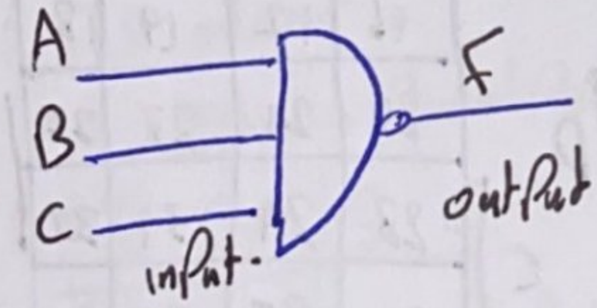
$f = A.B.C$.

2- OR Gates :-



$F = A + B + C$.

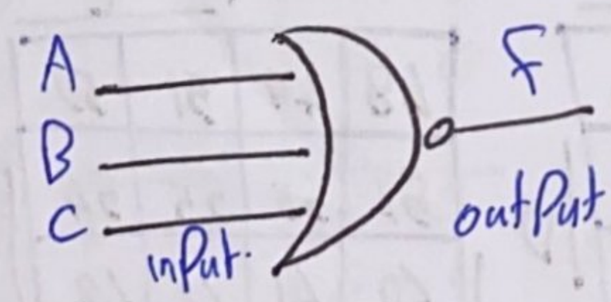
3- NAND Gates (AND Not Gates):-



$F = \overline{ABC}$

$F = \bar{A} + \bar{B} + \bar{C}$.

4- NOR Gates (OR Not Gates):-



$F = \overline{A + B + C}$

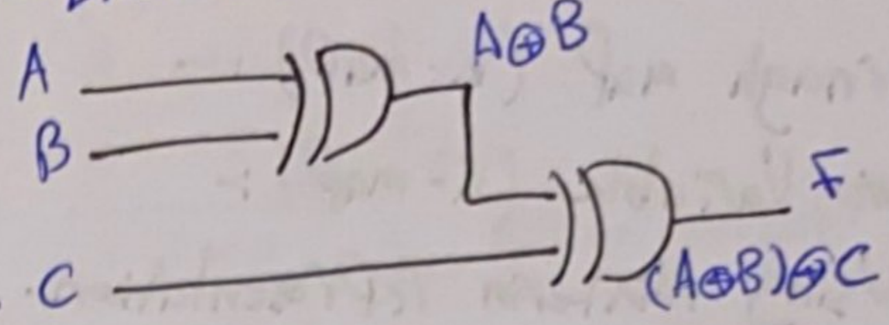
$F = \bar{A}\bar{B}\bar{C}$.

5- Exclusive OR Gates (XOR Gates):-

No Three or more input for (XOR) Gates Only Two input.

* logic Gates Three Input Gates :-

5- Exclusive OR Gates:-

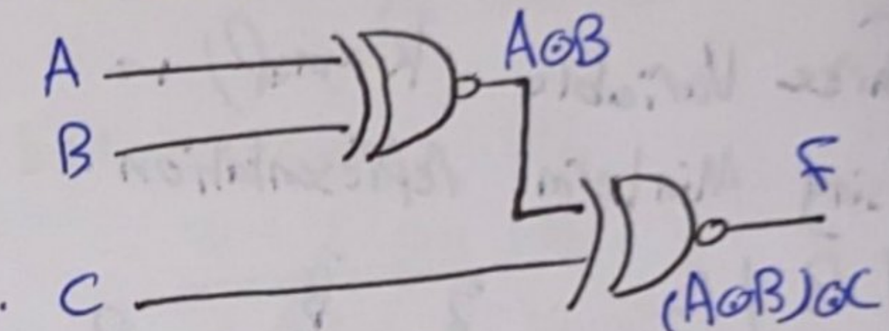


$F = (A \oplus B) \oplus C$.

$F = (A\bar{B} + \bar{A}B)\bar{C} + \overline{(A\bar{B} + \bar{A}B)}\,C$

$F = A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC$.

6- Exclusive NOR Gates (XNOR):-



$F = (A \odot B) \odot C$

$F = \overline{(A \odot B)}\,\bar{C} + (\bar{A}\bar{B} + AB)C$

$F = A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC$.

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* Minterms and maxterms :-

Num	Minterms		Maxterms	
0	$\bar{x}\bar{y}\bar{z}$	m_0	$x+y+z$	m_0
1	$\bar{x}\bar{y}z$	m_1	$x+y+\bar{z}$	m_1
2	$\bar{x}y\bar{z}$	m_2	$x+\bar{y}+z$	m_2
3	$\bar{x}yz$	m_3	$x+\bar{y}+\bar{z}$	m_3
4	$x\bar{y}\bar{z}$	m_4	$\bar{x}+y+z$	m_4
5	$x\bar{y}z$	m_5	$\bar{x}+y+\bar{z}$	m_5
6	$xy\bar{z}$	m_6	$\bar{x}+\bar{y}+z$	m_6
7	xyz	m_7	$\bar{x}+\bar{y}+\bar{z}$	m_7
	$x.y.z \rightarrow 1$		$\bar{x}.\bar{y}.\bar{z} \rightarrow 1$	
	$\bar{x}.\bar{y}.\bar{z} \rightarrow 0$		$x.y.z \rightarrow 0$	
	Sum of Product		Product of sum	

$F(x,y) = (\bar{x}+y)\cdot(\bar{x}+\bar{y}) = \Pi(2,3)$

$F(A,B) = AB + \bar{A}\bar{B} = \Sigma(0,3)$

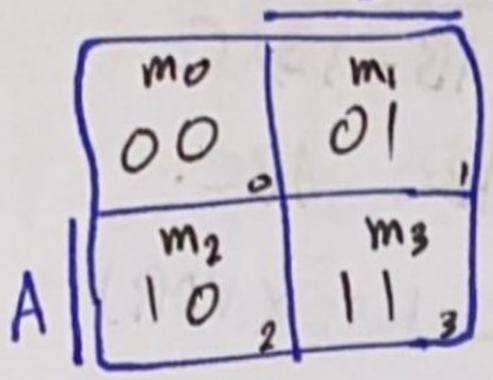
* Digital logic and Digital Electronics:-

* Logic Gates :-

* Karnagh map (K-map) :-

1- Two Variable (K-map) :-

Using Minterm representation.

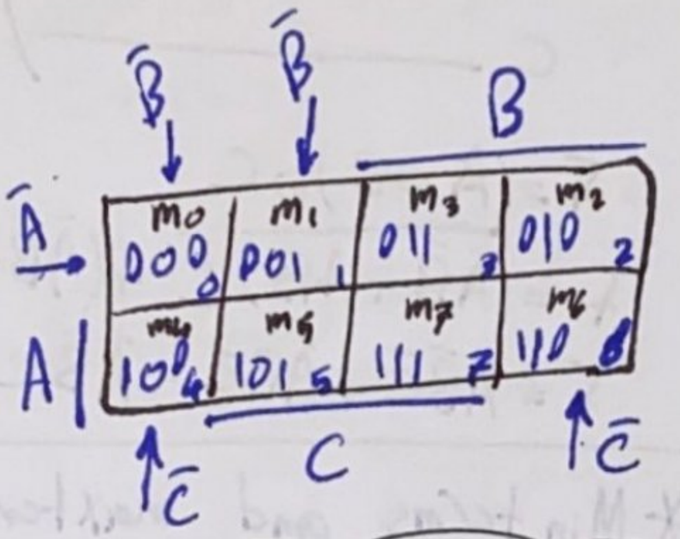


A	B
0	0
0	1
1	0
1	1

2- Three Variable (K-map) :-

Using Minterm representation.

A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

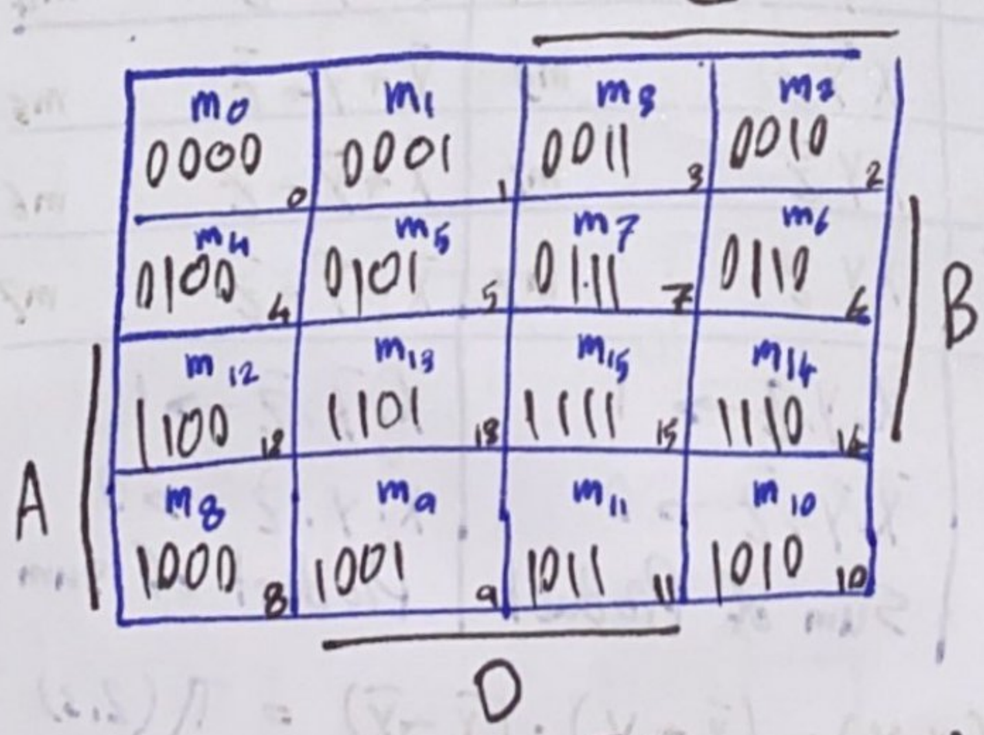


Three Variable K-map ⇒ Cylinder

four Variable K-map ⇒ sphere.

3- four Variable (K-map) :-

Using Minterm representation.



F(A,B,C,D) ⇔ F(W,X,Y,Z)

* Rules for K-map simplification

Using minterms :-

1- Cover all ones and non of Zeros.

2- Minimize the number of circles

3- Maximize size for every circles.

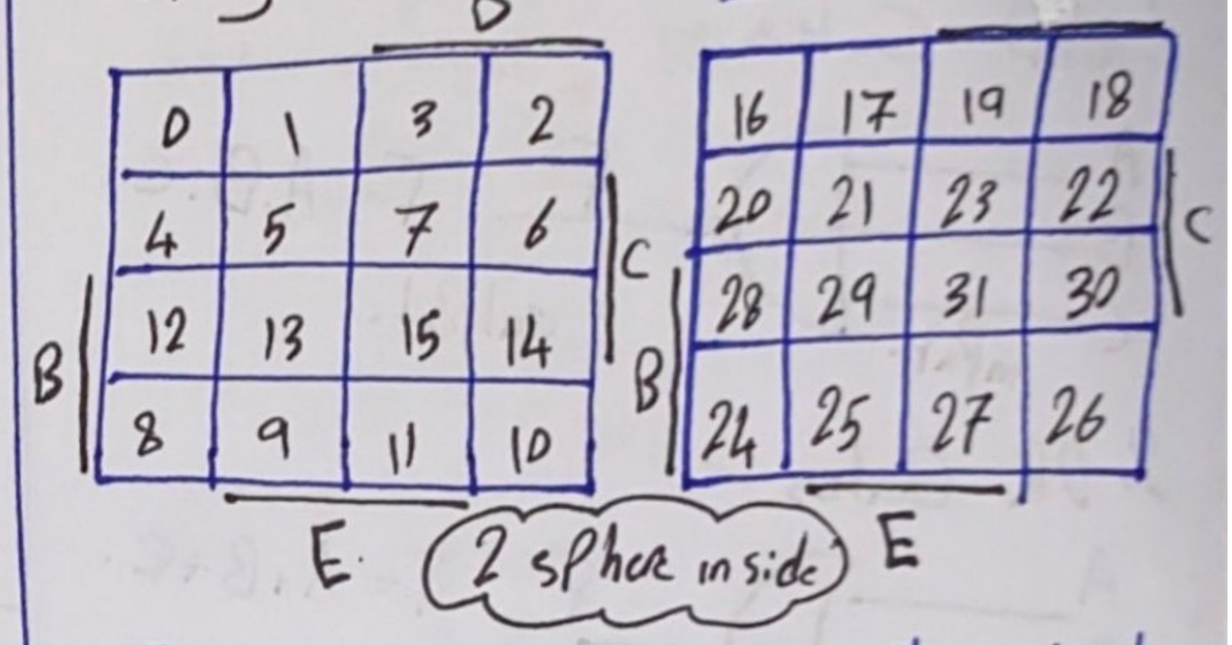
4- Every circle should be inclued

1, 2, 4, 8, 16 ones.

* Karnagh map (K-map) :-

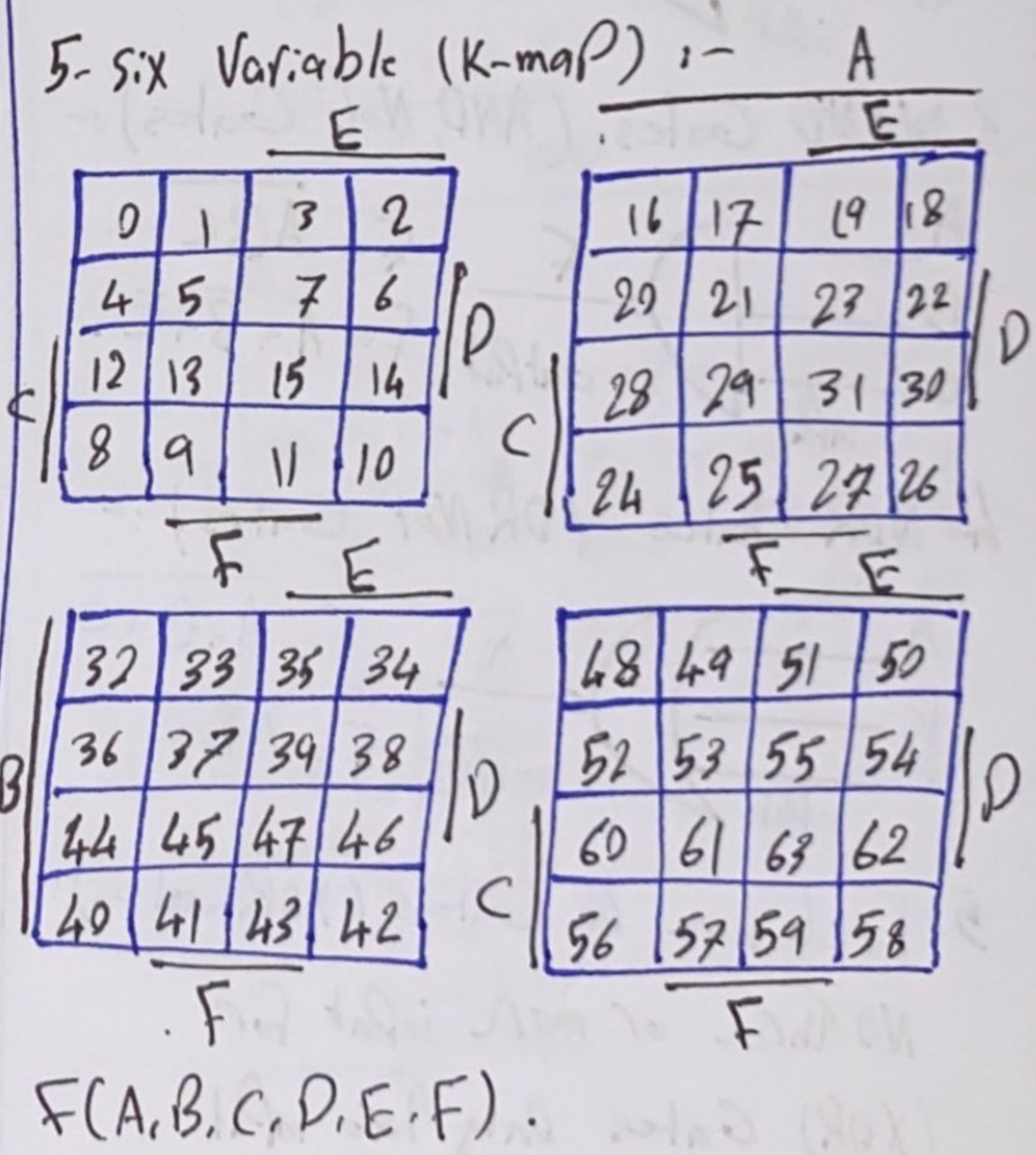
4- Five Variable (K-map) :-

Using minterm representation :- A



Five Variable K-map ⇒ 2 sphere inside

5- Six Variable (K-map) :-

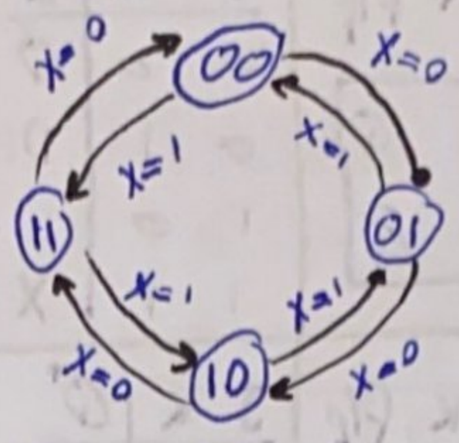


F(A,B,C,D,E,F).

Digital logic and Digital Electronics :-

* Design 2 bit up/down counter :-

A	B	X	F_1	F_2
0	0	0	0	1
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	0



$F_1 = A \oplus B \oplus X$

$F_2 = \bar{B}$.

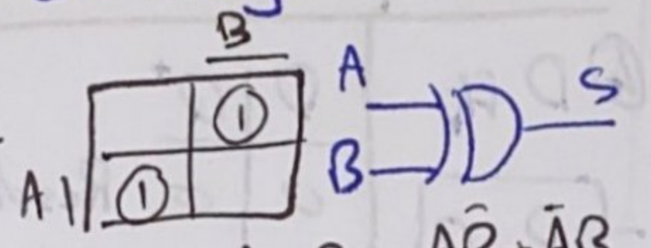
* Adder :-

1. Half adder :- (addition Two bits)

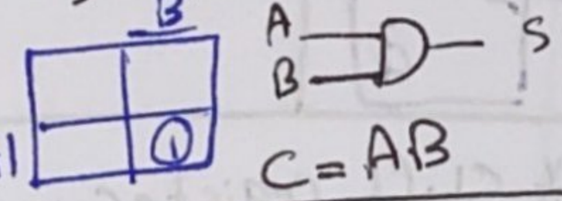
2 input → 2 output (S, C).

S → Sum . C → Carry.

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



$S = A \oplus B = A\bar{B} + \bar{A}B$



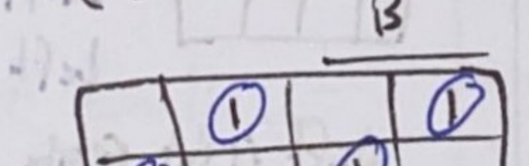
$C = AB$

* Adder :-

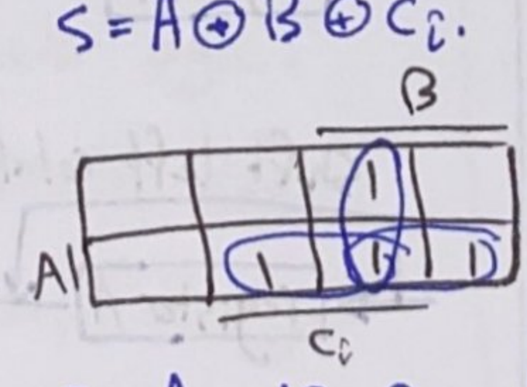
2- Full adder :-

3 input → 2 output (S, C).

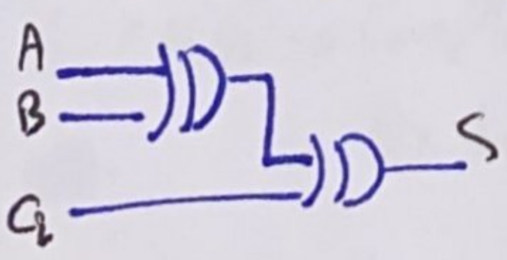
A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

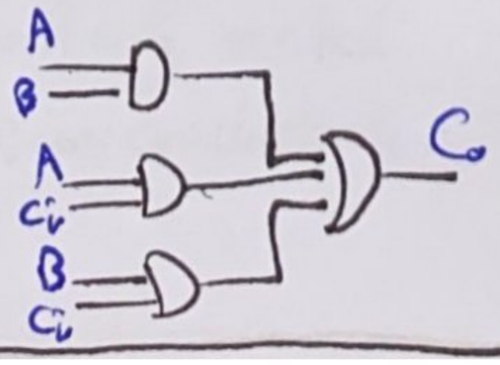


$S = A \oplus B \oplus C_i$.



$C_o = AC_i + AB + BC_i$





* BCD addition :-

1. Sum ≤ 9. ⇒ Answer is correct.

Ex: 0 0 1 0 $(2)_{10}$
+ 0 1 1 0 BCD $(6)_{10}$
1 0 0 0 $8_{(10)} \leq 9$ → correct.

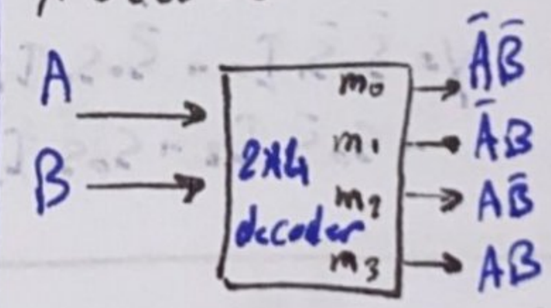
Ex: 0 0 1 1 $(3)_{10}$
+ 0 1 0 0 BCD $(4)_{10}$
0 1 1 1 BCD $(7)_{10} \leq 9$ → correct.

2. Sum > 9 ⇒ Answer is incorrect.
We add (6 = 0110).

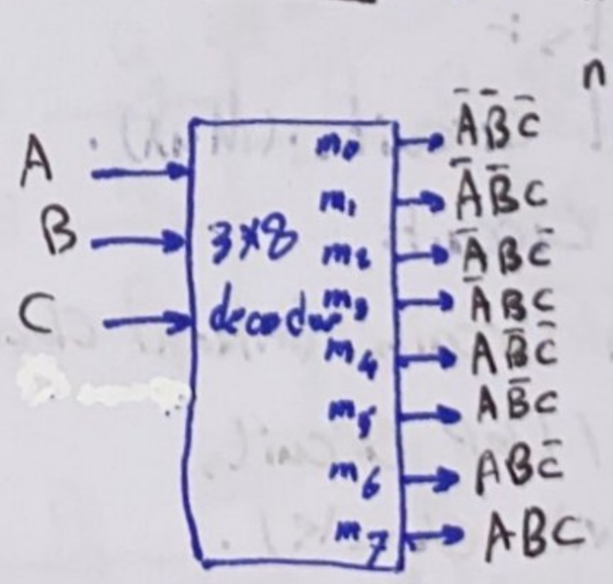
Ex: 1 1 1
0 0 1 1 $(3)_{10}$
+ 0 1 1 1 BCD $(7)_{10}$
1 0 1 0 $10_{10} > 9$
+ 0 1 1 0
1 0 0 0 0 BCD.

Ex: 1
1 0 0 0 $(8)_{10}$
+ 1 0 0 1 BCD $(9)_{10}$
1 0 0 0 1 $(17)_{10} > 9$.
+ 0 1 1 0
1 0 1 1 1 BCD

* Decoder :-



n=2 → output = 4
n=3 → output = 8
n=4 → output = 16
n=5 → output = 32

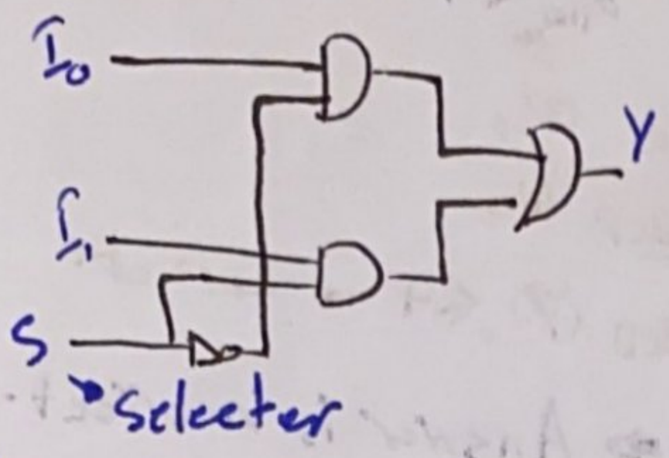


* Digital logic and Digital Electronics :-

* Design with Multiplexer (MUX) :-

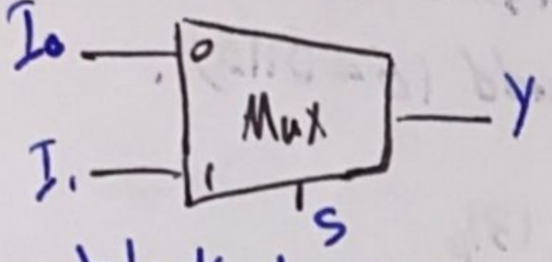
Multipule input → one output.

1. 2 input multiplexer :-



logic diagram (2*1) Mux

S	Y
0	I_0
1	I_1

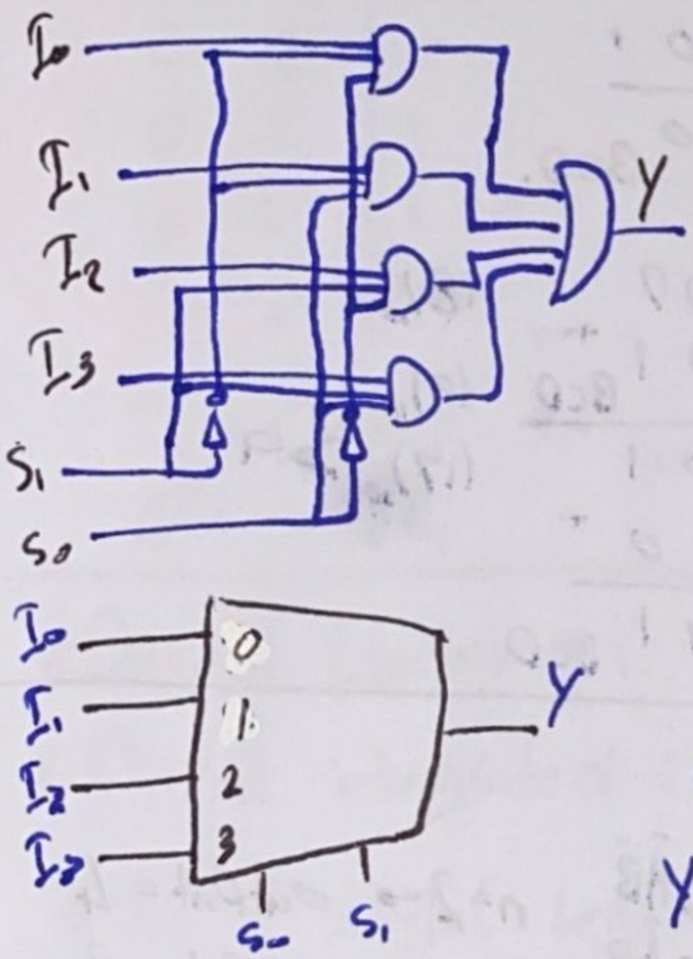


block diagram

Characteristic equ

$$Y = I_0 \bar{S} + I_1 \cdot S$$

2. 4 input multiplexer :-



logic diagram (4*1) mux

S_0	S_1	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

block diagram

Characteristic equ

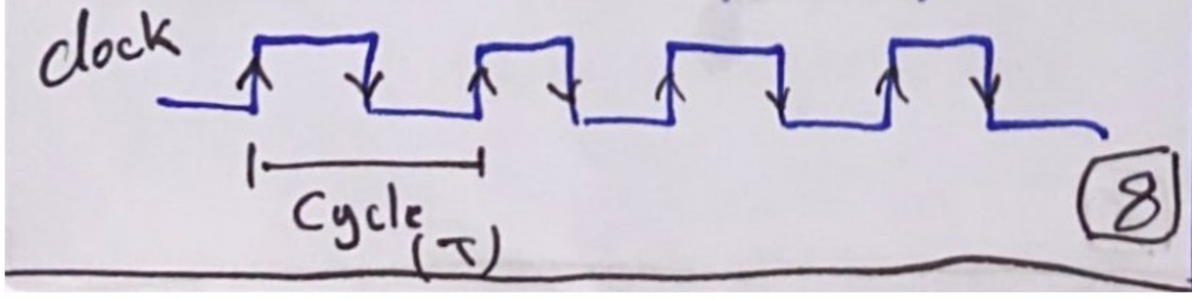
$$Y = \bar{S}_0 \bar{S}_1 I_0 + \bar{S}_0 S_1 I_1 + S_0 \bar{S}_1 I_2 + S_0 S_1 I_3$$

* Digital Circuits :-

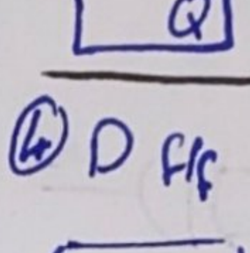
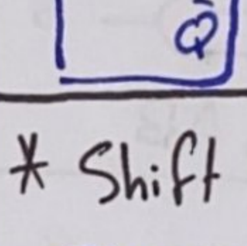
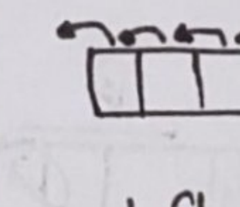
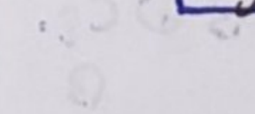
1. Combinational Circuits. (Mux).
2. Sequential Circuits :-

like :- 1. latch Circuits (without Clock)

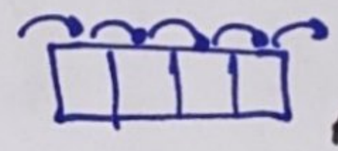
2. Flip / Flop Circuits (with Clock).

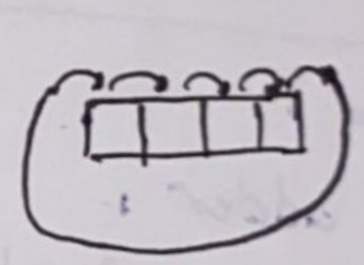


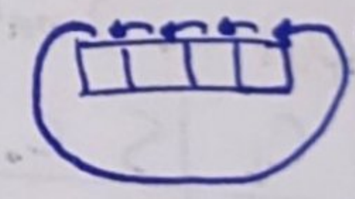
* Flip / Flop Circuits :-

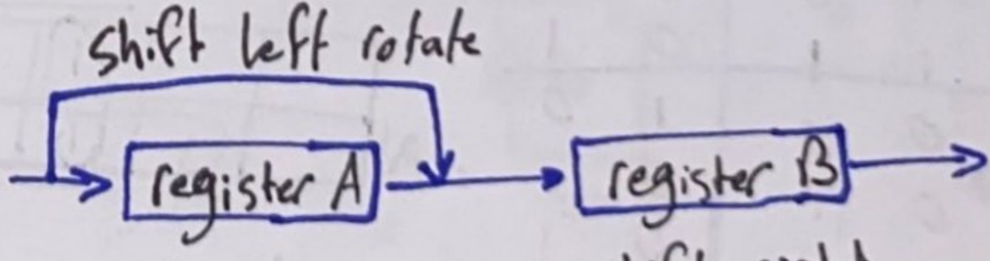
Name	state table	characteristic equ
① SR flip flop 	S R | Q^+ 0 0 | Q No change 0 1 | 0 Reset 1 0 | 1 set 1 1 | X invalide	X
② JK flip flop 	J K | Q^+ 0 0 | Q No Change 0 1 | 0 Reset 1 0 | 1 set 1 1 | $\bar{Q}$ Toggle	$Q^+ = J\bar{Q} + \bar{K}Q$
③ T flip flop 	T | Q^+ 0 | Q No change 1 | $\bar{Q}$ Toggle	$Q^+ = T \oplus Q$ $= T\bar{Q} + \bar{T}Q$
④ D flip flop 	D | Q^+ 0 | 0 Reset 1 | 1 set	$Q^+ = D$

* Shift register :-









* Digital Logic and Digital Electronics :-

* Digital logic :-

* Excitation Tables :-

1- Excitation tables of D_{flf}

Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

$D = Q^+$

2- Excitation table of JK flf.

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

$Q^+ = J\bar{Q} + \bar{K}Q.$

3- Excitation table of T_{flf}.

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

$T = Q \oplus Q^+$

$Q^+ = T \oplus Q$

* Digital Electronics :-

* Digital Integrated circuits :-

* The IC digital logic families :-

1- RTL → Resistor Transistor logic.

2- DTL → Diode Transistor logic.

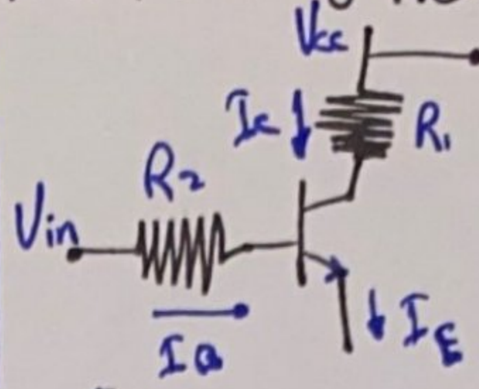
3- TTL → Transistor Transistor logic.

4- ECL → Emitter - Coupled logic.

5- MOS → Metal Oxide semiconductors

6- CMOS → Complementary metal Oxide semiconductors

* Bi Polar Junction Transistor (BJT) :-



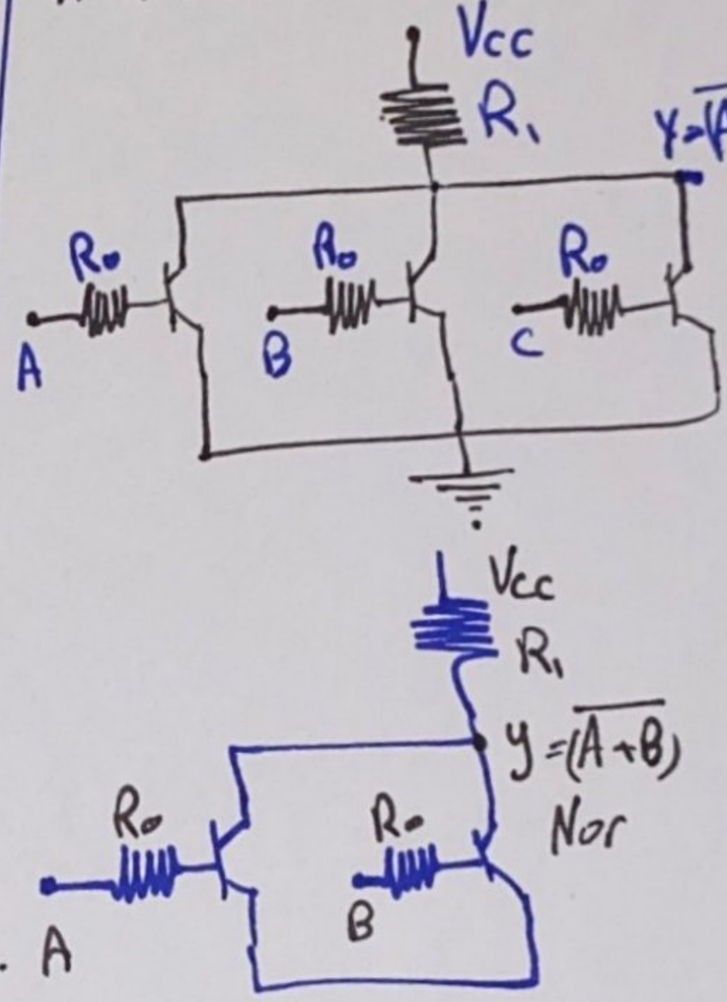
$I_E = I_c + I_B$

$I_c = \beta I_B$.

* Typical NPN silicon Transistor Parameter

Region	V_{BE}	V_{CE}	Current Relation
Cutt-off	< 0.6	open circ	$I_B = I_c = 0$.
Active	0.6 - 0.7	> 0.8	$I_c = \beta I_B$
Saturation	0.7 - 0.8	0.2	$I_B \geq \frac{I_c}{\beta}$

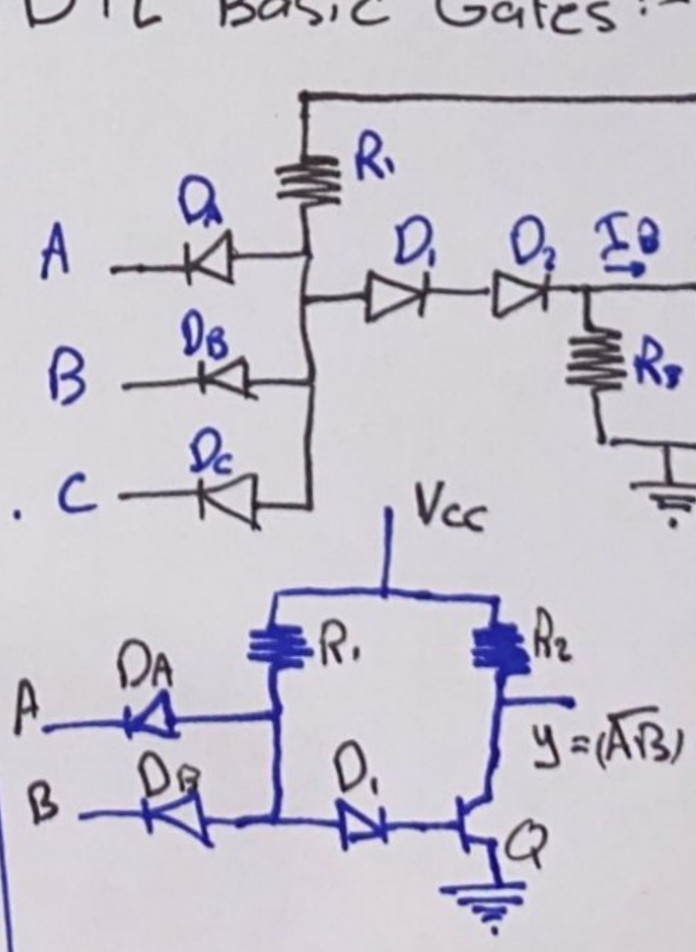
* RTL Basic Gates :-



A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

A	B	y
0	0	1
0	1	0
1	0	0
1	1	0

* DTL Basic Gates :-



A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0